ISC0701
128 Channel
Flat Panel X-ray ROIC

Specification

400-0701-09 VERSION 3.00

Document Revision History

- **Version 3.00, August 31, 2012**
  - Initial Release

ISC0701 General Description

- **128 channels**
- **80um channel pitch**
- **Die size: 11.15mm by 4.32mm, excluding scribe**
- **Charge amp / column**
  - Charge integrator architecture
  - Programmable gain
- **Low pass filter**
  - Adjustable time constant
- **Correlated double sampling**
- **On-chip ADC**
  - 12 to 14 bits slope converter
- **Line timing modes**
  - Read then clamp (RTC) or read while clamp (RWC)
- **Serial control interface**
  - Single command word controls all settings
- **LVDS interface (input/ output)**

ISC0701 Nominal Detector Array Characteristics

ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Photodiode Capacitance	0.5pF – 2.5pF (typical 1.6pF)	$C_{PHOTODIODE}$
Photodiode Dark Current @ 20°C	1fA – 6fA (typical 3fA)	
Photodiode Dark Current @ 60°C	180fA	
Data Line Capacitance	20pF – 100pF (typical 30pF)	
Data Line to Data Line Capacitance	$\leq$ 0.05pF/cm	28cm length → $\leq$ 1.4pF
Data Line Series Resistance	0.5kΩ – 2kΩ (typical 1kΩ)	
TFT R_{ON}	$\leq$ 2MΩ (typical 1MΩ)	
Signal Time Constant	$\leq$ 5us	$R_{ON} * C_{PHOTODIODE}$
TFT Gate-source/drain Capacitance	$\leq$ 40fF (typical 25fF)	
TFT Gate Capacitance	80fF	TFT threshold ~ 8V Includes gate-source/drain capacitance
TFT Gate Voltage Swing	$\leq$ 25V (typical 22.5V)	-7.5V to 15V
TFT gate control signal time constant	$\leq$ 1.2us (typical 0.8us)	
Defects	Open gate line Open data line Shorted data line Shorted pixel	See fault tolerance analysis

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Input DC Offset	1.0 to 3.5V (nominal 1.2V)	Adjustable integrator DC operating point
Carrier Collected	Electrons	
Input Charge Handling	≥ 15pC	Normal operation
Input Charge Handling	≥ 200pC	Reset mode
Readout Noise	ENC ≤ 800e- ≤ 950e- ≤ 1100e- ≤ 1300e- ≤ 2000e- ≤ 3000e-	CINT CDET TAU RES ΔV 0.25pF 30pF 3.7us 13bit 1.5V 0.25pF 30pF 2.3us 13bit 1.5V 0.50pF 30pF 2.3us 13bit 2V 1.00pF 30pF 2.3us 14bit 2V 2.00pF 30pF 2.3us 14bit 4V 4.00pF 30pF 5.0us 14bit 4V Does not include system or detector contributions
Integrator Gain Control	C_{INT} = 0.25pF – 4pF, 0.25pF increments	
Gain Ratio Accuracy	≤ +/–5%	
LPF Time Constant	1us, 2.3us, 3.7us, 5us ±20%	
ROIC Crosstalk	≤ 0.5%	
PSRR	≥ 30dB	

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Power Dissipation	≤ 190mW	
Frame Rates 2000 lines, digital	≥ 7.2Hz ≥ 6Hz ≥ 2Hz	12 bit ADC, ≤ 69us / line 13 bit ADC, ≤ 83us / line 14 bit ADC, ≤ 250us / line
Clock Frequency	85MHz	
# Of Channels	128	
Channel Pitch	80um	
Input Biases	VPOS 5.5V VNEG 0.0V VPOSR 5.5V VNEGR 0.0V VNEGADC 0.0V VPOSD 5.5V VPD 3.3V/2.5V VND 0.0V VREF_INT 1.2V (nom) VREF_CDS 0.5V (nom) VREF_ADC 0.5V (nom) VREF_RAMP 4.5V (nom)	Analog Positive Analog Negative Analog Positive (for ramp circuitry) Analog Negative (for ramp circuitry) Common Reference for Ramp, T/H Digital Positive Digital Positive Digital Negative Integrator Reference CDS Reference ADC Reference Ramp Gain Adjust
Input Clocks	Name VIC VID CLK 1.25V 0.35V SYNC 1.25V 0.35V DATA 1.25V 0.35V	V_{IC} range: 0.8-1.6V, V_{ID} range: 0.1-0.6V Master Clock Sync Mode Control
Die Size	11.15mm x 4.74mm or smaller	Based on existing size of ISC9717 Actual size: 11.15mm x 4.32mm

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ROIC PARAMETER	SPECIFICATION REQUIREMENT	COMMENTS
Operating Temperature	10°C – 70°C	At ROIC
ADC Resolution	12, 13, 14 bits	
Channel Nonlinearity	≤ 1.0%	From 500 to 15,000 counts (3% to 92%)
Channel-Channel Nonlinearity	≤ 0.5%	
Offset correction error over full dynamic range	< 1%	or < 1LSB if signal is < 100LSB
Offset stability	< 0.5LSB/°C	C_{INT} = 2pF
Number Of Outputs	2	
Digital Output Settling	≤ 4.0ns for 10%-90%	30pF, 100Ω termination
Digital Readout Rate	≥ 85MHz	2 outputs → 170MHz data throughput rate